REMARKS

Applicants affirm the species election of claims 1-12 and 15-18. Claims 13-14 are withdrawn from consideration as being drawn to non-elected species.

The drawings are objected to under 37 CFR 1.83 for reasons stated in the Office Action at page 2, second paragraph. The drawings are amended to show solder bumps. In particular, Figure 2 is amended to show solder bumps 215, Figure 4 is amended to show solder bumps 415, Figure 6 is amended to show solder bumps 615, and Figure 8 is amended to show solder bumps 815. In addition, the specification at page 6, lines 30-31 is amended to refer to solder bumps 215, page 7, line 13 is amended to refer to solder bumps 415, page 8, line 14 is amended to refer to solder bumps 415, page 9, lines 25-26 is amended to refer to solder bumps 615, page 10, line 8 is amended to refer to solder bumps 815, and page 11, line 8 is amended to refer to solder bumps 815. Therefore, solder bumps 215 are shown in Figure 2 of the drawings, and are also referenced in the amended specification. Solder bumps 415 are shown in Figure 4 of the drawings, and are also referenced in the amended specification. Solder bumps 615 are shown in Figure 6 of the drawings, and are also referenced in the amended specification. Solder bumps 815 are shown in Figure 8 of the drawings, and are also referenced in the amended specification. No new matter is added. Amended Figures 2, 4, 6, and 8 are also attached hereto to replace previously submitted Figures 2, 4, 6, and 8. A marked-up version of Figures 2, 4, 6, and 8 of the drawings, with revisions shown in red, is included with the amended drawings. Reconsideration of the objections to the drawings is respectfully requested.

Claims 1-12 and 15-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The claims are amended above in a manner believed to overcome the rejections. Entry of the amendments and removal of the rejections are respectfully requested.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Corisis (U.S. Patent Number 6,607,937). Claims 2-4, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis in view of Bolkin, *et al.* (U.S. Patent Number 6,798,057). Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Bolkin, *et al.* and further in view of Koh, *et al.* (U.S. Patent Number 6,737,738). Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, and Koh, *et al.* and further in view of

Yanagida (U.S. Publication Number 2001/0042923) and Jiang, *et al.* (U.S. Patent Number 6,906,415). Claims 10-12 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references.

The present invention as claimed is directed to a multi-chip package comprising a first semiconductor chip, at least one second semiconductor chip, a first connecting unit, and a second connecting unit. The at least one second semiconductor chip is in a wafer level configuration and is stacked on the first semiconductor chip via stacking means. A back surface of the first semiconductor chip abuts a back surface of the second semiconductor chip. The first connecting unit is attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system. A second connecting unit is attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system.

Claim 1 is amended herein to clarify certain details of the invention. In particular, claim 1 is amended to specifically point out that a back surface of a first semiconductor chip abuts a back surface of a second semiconductor chip. In addition, claim 1 is amended to point out that a first connecting unit is attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system, and a second connecting unit is attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system.

With regard to the rejection of claim 1, it is submitted that Corisis fails to teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed. Instead, Corisis teaches a packaged device 420 comprising a first microelectronic die 424a (referred to in the Office Action as a first semiconductor chip) that is encased in a first encapsulating material 423a (see Corisis, Figure 5 and column 5, lines 63-67). A second microelectronic die 424b is mounted to the surface of the first encapsulating material 423 of the packaged device 420 (see Corisis, Figure 5 and column 6, lines 3-5). There is no mention in Corisis of a back surface the first microelectronic die 424a abutting a back surface of the second microelectronic die 424b. It therefore follows that the first microelectronic die of

Corisis is not the Applicants' claimed first semiconductor chip, and the second microelectronic die of Corisis is not the Applicants' claimed second semiconductor chip.

It therefore follows that Corisis fails to teach or suggest the present invention, as claimed in amended independent claim 1. Reconsideration and removal of the rejection of claim 1 under 35 U.S.C. 102(e) based on Corisis are respectfully requested.

With regard to the rejection of claims 2-4, 9 and 15 under 35 U.S.C. 103(a) over Corisis in view of Bolkin, *et al.*, it is submitted that Bolkin, *et al.*, like Corisis, fails to teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed. Instead, Bolkin, *et al.* teaches first and second dies 102, 104 that are each mechanically bonded to an interposer 101 (see Bolkin, Figure 1 and column 2, lines 55-59).

It is therefore submitted that neither Corisis, *et al.* nor Bolkin, *et al.* teaches or suggests elements of the claims set forth above. Specifically, neither reference teaches or suggests a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed.

Since neither Corisis, *et al.* nor Bolkin, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Corisis, *et al.* and Bolkin, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 2-4, 9 and 15 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of 2-4, 9 and 15 under 35 U.S.C. 103(a) based on Corisis, *et al.* and Bolkin, *et al.* is respectfully requested.

With regard to the rejection of claim 5 under 35 U.S.C. 103(a) over Corisis, Bolkin, *et al.* and Koh, *et al.*, it is submitted that Koh, *et al.*, like Corisis and Bolkin, *et al.*, fails to teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed. Instead, Koh, *et al.* teaches a first IC package 22 and a second IC package 24 that are separated from each other by an airspace 23 (see Koh, Figure 2 and column 4, lines 24-30).

It is therefore submitted that none of the Corisis, Bolkin, *et al.*, and Koh, *et al.* references teaches or suggests elements of the claims set forth above. Specifically, none of the references teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed.

Since none of the Corisis, Bolkin, *et al.*, and Koh, *et al.* references teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Corisis, Bolkin, *et al.*, and Koh, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claim 5 is believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claim 5 under 35 U.S.C. 103(a) based on Corisis, *et al.*, Bolkin, *et al.*, and Koh, *et al.* is respectfully requested.

With regard to the rejection of claims 6-8 under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.*, it is submitted that Yanagida and Jiang, *et al.*, like Corisis, Bolkin, *et al.*, and Koh, *et al.*, fail to teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed.

It is therefore submitted that none of the Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.* references teaches or suggests elements of the claims set forth above. Specifically, none of the references teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed.

Since none of the Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.* references teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 6-8 are believed to be allowable over the cited references. Accordingly, reconsideration

of the rejection of claims 6-8 under 35 U.S.C. 103(a) based on Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.* is respectfully requested.

With regard to the rejection of claims 10-12 and 16-18 under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.*, it is submitted that none of the Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* references teaches or suggests a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed. Specifically, none of the references teach or suggest a back surface of a first semiconductor chip abutting a back surface of a second semiconductor chip, as claimed.

Since none of the Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* references teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 10-12 and 16-18 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejection of claims 10-12 and 16-18 under 35 U.S.C. 103(a) based on Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 2/8/06

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Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 2, 4, 6, and 8. The sheets, which includes Figures 2, 4, 6, and 8, replace the original sheets. Specifically, Figure 2 is amended to include solder bumps 215, which were missing from the original sheet. In addition, Figure 4 is amended to include solder bumps 415, which were missing from the original sheet. In addition, Figure 6 is amended to include solder bumps 615, which were missing from the original sheet. In addition, Figure 8 is amended to include solder bumps 815, which were missing from the original sheet.

A marked-up version of the drawings, with revisions shown in red, is included with the amended drawings. Entry of the amendments to the drawings is respectfully requested.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

FIG. 2

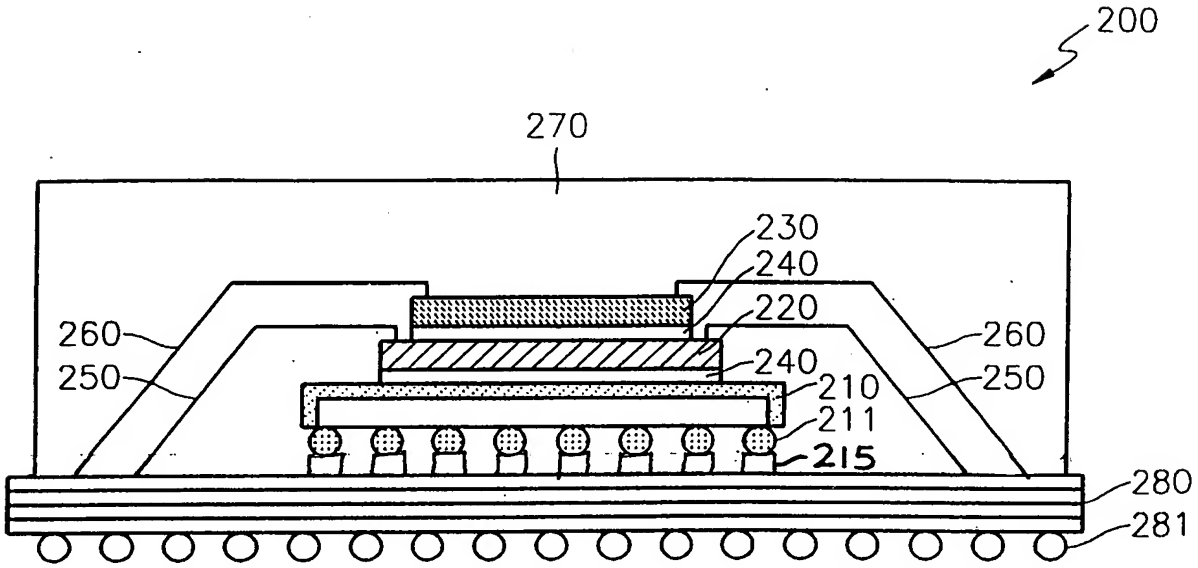
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FIG. 3

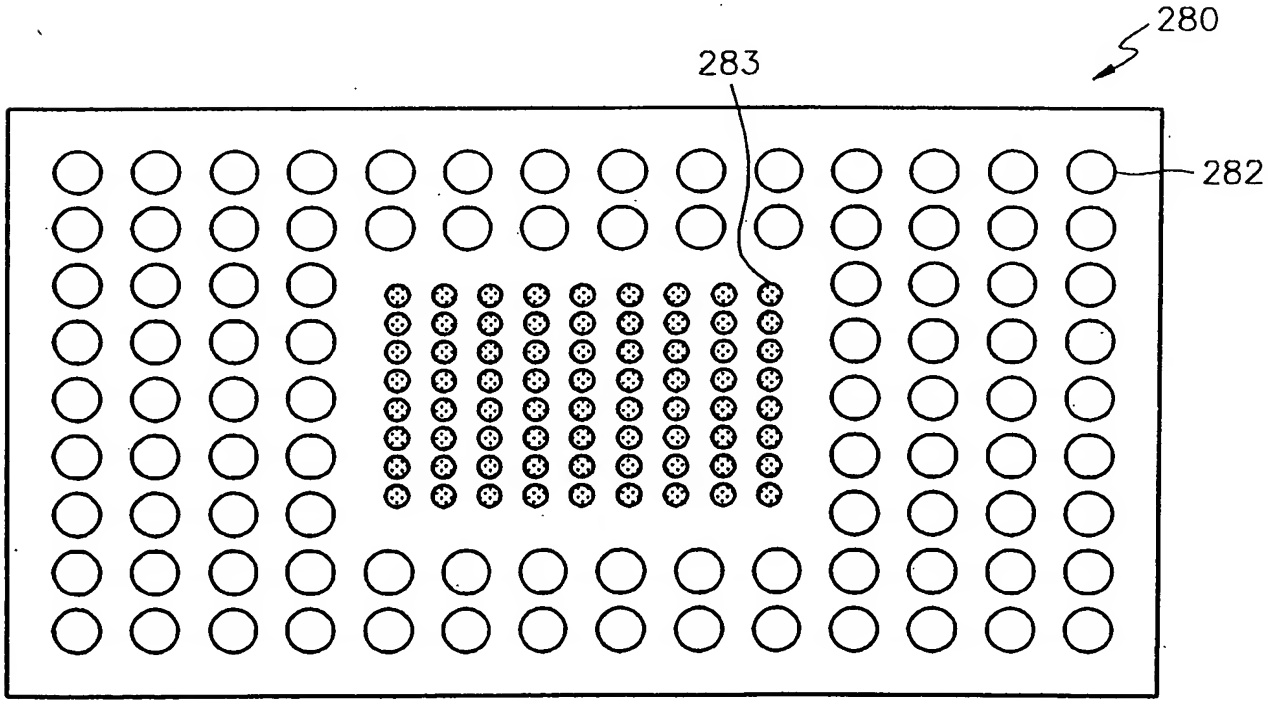
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FIG. 4

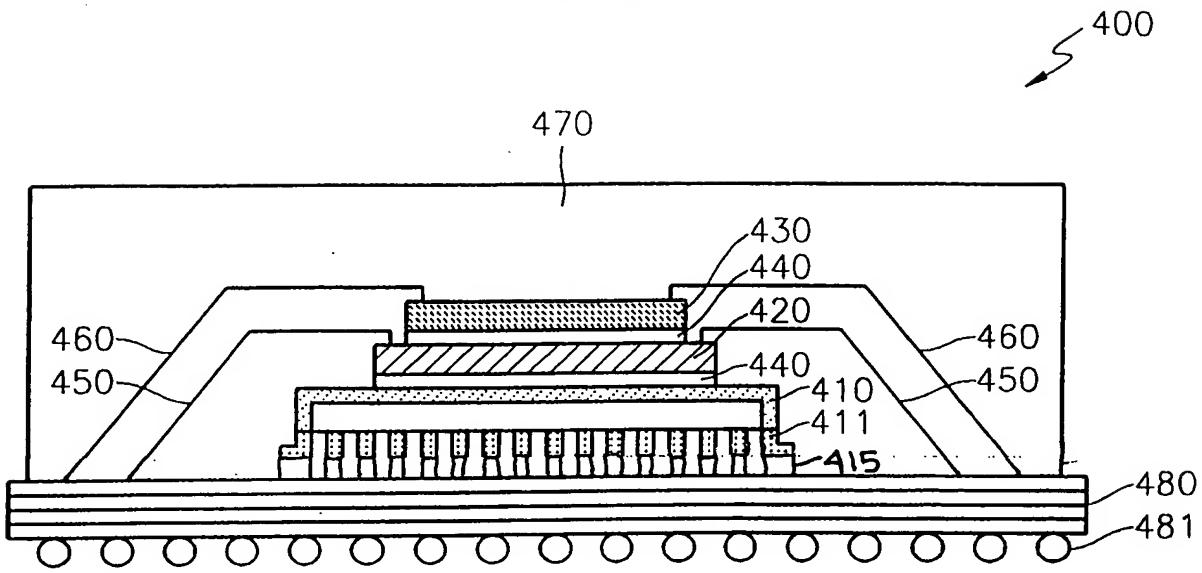
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FIG. 5

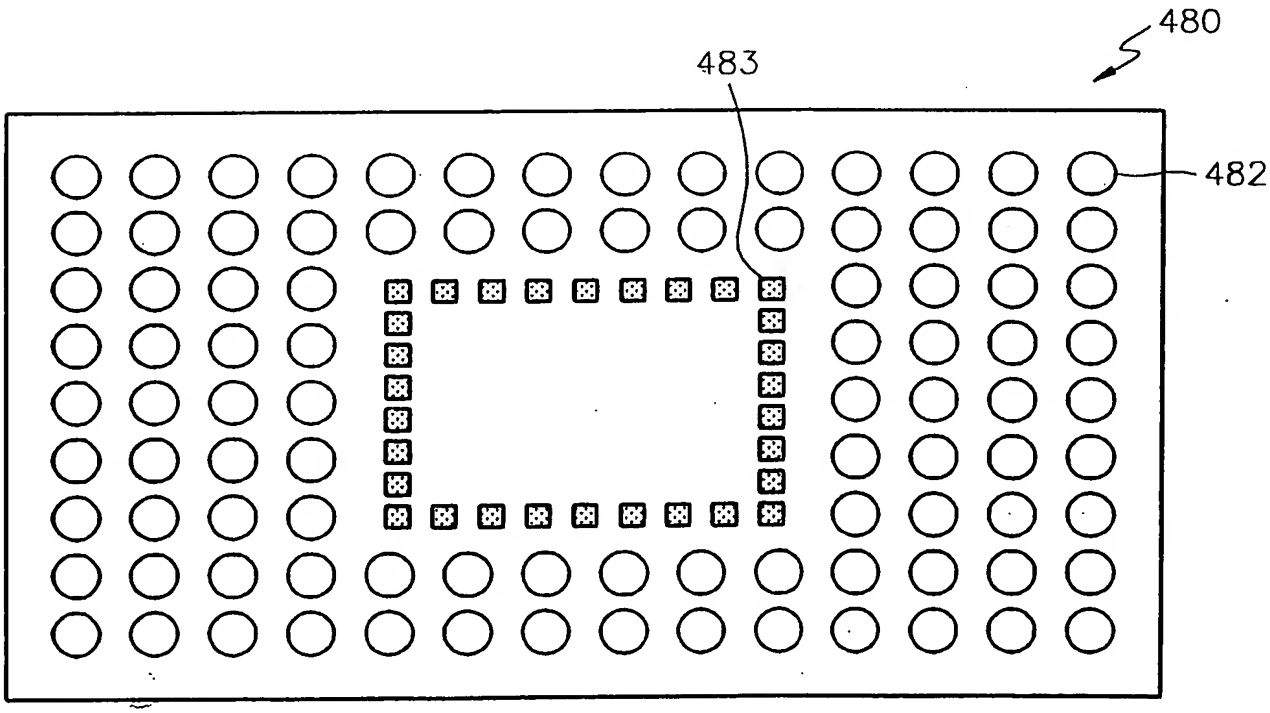
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FIG. 6

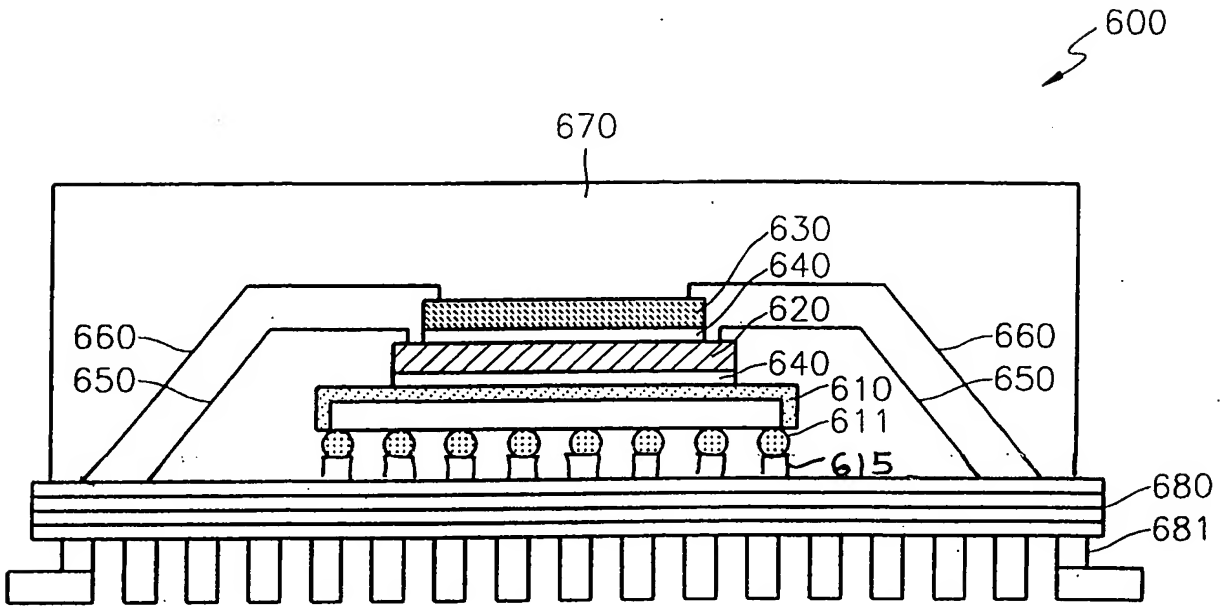
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FIG. 7

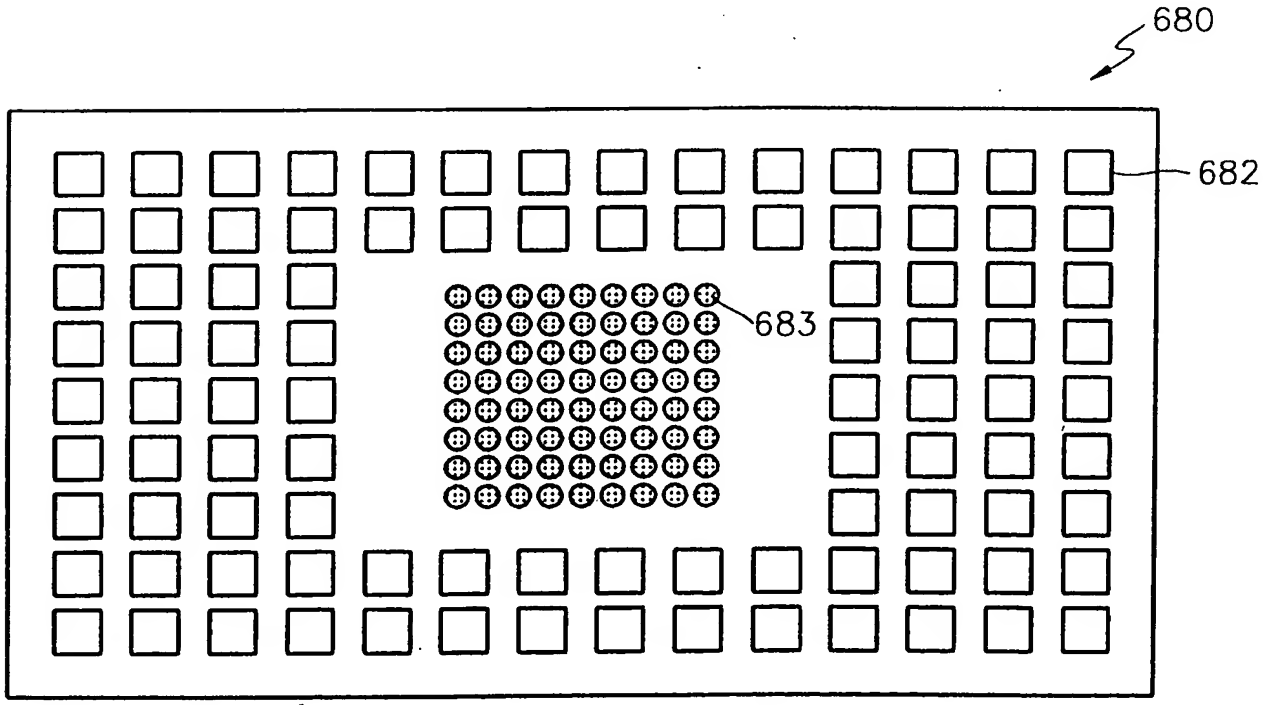
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FIG. 8

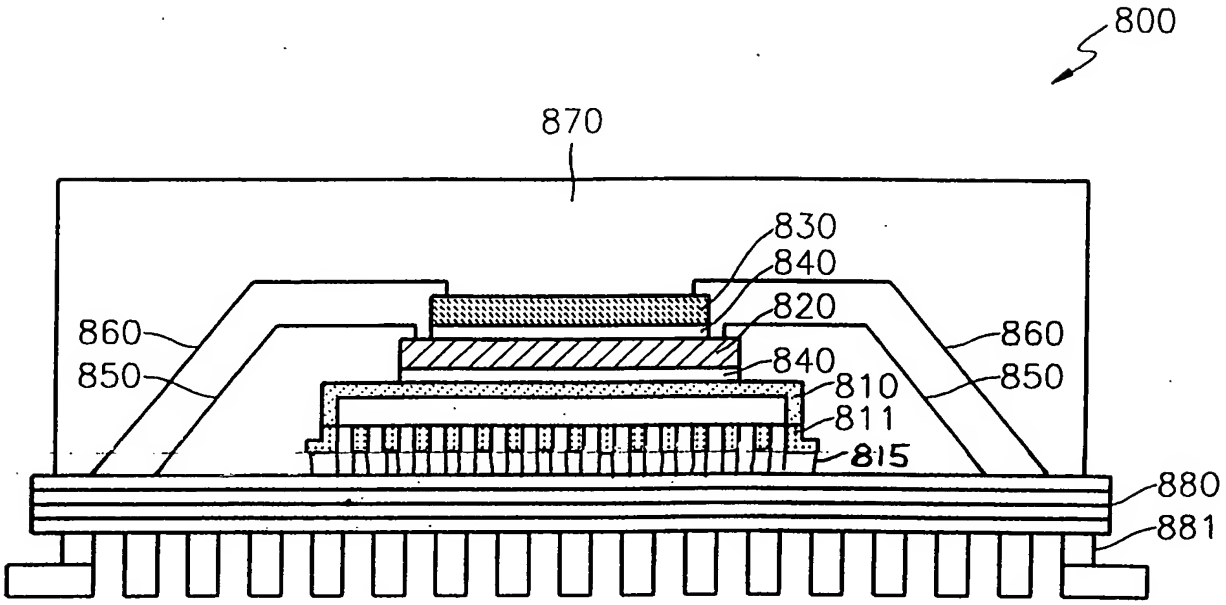
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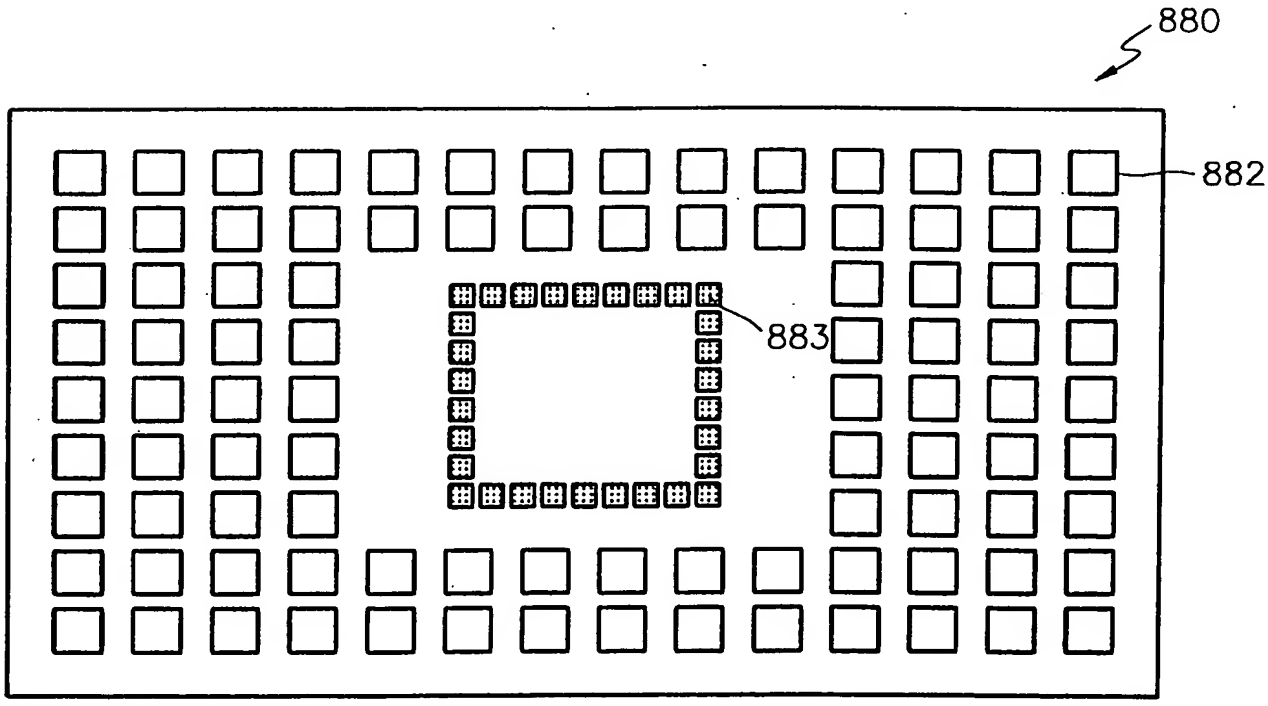
FIG. 9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